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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,752	12/20/2000	Vincent Chen	1875.0220000	4979

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,752	CHEN ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-22* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 20-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 recites the limitation "opposing said first side" in line 9. There is insufficient antecedent basis for this limitation in the claim. The examiner suggests the following changes:

"a second switch transistor connected between a second [side] terminal of said capacitor opposing said first [side] terminal and a second voltage."

Claim 21 is rejected due to their dependency on claim 20.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5-10, 12-14, 17-18 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Karp et al. (US Pat. No. 6,266,269 B1).

Regarding claim 1, Karp et al. teaches a one-time programming memory element comprising: a capacitor (303) (see Fig. 3A) having an oxide capable of passing direct gate tunneling current (see col. 6, lines 51-53); a write switch (302) (see fig. 3A) including plural transistors (consider the transistors (302) in each memory cells 301(1,1)...(1-4) along WWL (1) in fig. 3B) each having a gate oxide layer that is thicker than said capacitor oxide layer (see col. 6, lines 30-40); and a read switch (304 and 141(1)...(4)) (see fig. 3B), including plural transistors (304 and 141(1)...(4)) (see fig. 3B) coupled to said capacitor (303) (see fig. 3B), each read switch transistor having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer (see col. 6, lines 30-40), wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less (see col. 6, lines 50-52 and col. 7, lines 15-24).

Regarding claim 8, Karp et al. teaches a one-time programming memory element comprising: a capacitor (303) (see Fig. 3A) having an oxide capable of passing direct gate tunneling current (see col. 6, lines 51-53); a write switch (302) (see fig. 3A) including plural transistors (consider the transistors (302) in each memory cells 301(1,1)...(1-4) along WWL (1) in fig. 3B) each having a gate oxide layer that is thicker than said capacitor oxide layer (see col. 6, lines 30-40); and a read switch (304) (see fig. 3A), including plural transistors (consider the transistors (304) in each memory cells

301(1,1)...(1-4) along RWL (1) in fig. 3B), each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer (see col. 6, lines 30-40), wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less (see col. 6, lines 50-52 and col. 7, lines 15-24).

Regarding claim 18, Karp et al. teaches a one-time programming memory element comprising: a capacitor (303) (see Fig. 3A) having an oxide layer, approximately 20 Å thick (see col. 6, lines 38-40), capable of passing direct gate tunneling current (see col. 6, lines 51-53); a write switch (302) (see fig. 3A) including plural transistors (consider the transistors (302) in each memory cells 301(1,1)...(1-4) along WWL (1) in fig. 3B) each having a voltage tolerance higher than that of said capacitor (consider the fact the gate oxide of the write switch is thicker than the gate oxide of the capacitor 303, see col. 6, lines 30-40); and a read switch (304 and 141(1)...(4)) (see fig. 3B), including plural transistors (304 and 141(1)...(4)) (see fig. 3B) coupled to said capacitor (303) (see fig. 3B), each read switch transistor having a voltage tolerance higher than that of said capacitor (consider the fact the gate oxide of the read switch is thicker than the gate oxide of the capacitor 303, see col. 6, lines 30-40), wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive

path having resistance of approximately hundreds of ohms or less (see col. 6, lines 50-52 and col. 7, lines 15-24).

Regarding claims 2 and 9, Karp et al. teaches that the capacitor oxide layer is approximately 20 Å thick (see col. 6, lines 38-40).

Regarding claims 3 and 10, Karp et al. teaches that the capacitor (303) comprises a FET having source (S) and drain (D) regions coupled to ground (see fig. 3A), a gate coupled to said write switch (302) (see fig. 3A) and a gate dielectric (203) forming said oxide layer (see fig. 2A and col. 6, lines 38-40).

Regarding claims 5, 12 and 17, Karp et al. teaches that said write switch comprises a 5-volt tolerant switch having a plural 2.5-volt transistors and wherein the voltage is less than 7 volts (see col. 8, lines 58-61).

Regarding claims 6-7 and 13-14, Karp et al. teaches a sensing circuit (120, 130, 343) to sense whether the capacitor is programmed (see Fig. 3B).

Regarding claim 22, Karp et al. teaches that when said write switch transistors (consider the transistors (302) in each memory cells 301(1,1)...(1-4) along WWL (1) in fig. 3B) are closed and said read switch transistor (see 304 and 141(1)...(4) in fig. 3B) are open, one-time programming occurs (see Table 3); and when said read switch transistors are closed and said write switch transistors are open, reading occurs (see Table 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4, 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al. (US Pat. No. 6,266,269 B1) in view of Kim et al. (US 2001/0022746 A1).

Regarding claim 4, 11 and 19, Karp et al. teaches a one-time programming memory element comprising: a capacitor (303) (see Fig. 3A) having an oxide capable of passing direct gate tunneling current (see col. 6, lines 51-53); a write switch (302) (see fig. 3A) including plural transistors (consider the transistors (302) in each memory cells 301(1,1)...(1-4) along WWL (1) in fig. 3B) each having a voltage tolerance higher than that of said capacitor (consider the fact the gate oxide of the write switch is thicker than

the gate oxide of the capacitor 303, see col. 6, lines 30-40); and a read switch (304 and 141(1)...(4)) (see fig. 3B), including plural transistors (304 and 141(1)...(4)) (see fig. 3B) coupled to said capacitor (303) (see fig. 3B), each having a voltage tolerance higher than that of said capacitor (303) (see col. 6, lines 30-40), wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less (see col. 6, lines 50-52 and col. 7, lines 15-24).

However, Karp et al. fails to teach that the capacitor includes a FET having a P-well layer, a deep N-well layer and a P-type substrate. Kim et al. teaches that is well known in the art to form a capacitor or antifuse comprising a FET (140) having a P-well layer (120) adjacent to the source and drain regions (130A-B), a deep N-well layer (110) below the P-well layer; and a P-type substrate (100) below the deep N-well layer (see Figs. 4A and 6A).

Karp et al. and Kim et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the capacitor/antifuse comprising a field effect transistor having a P-well layer adjacent to the source and drain regions, a deep N-well layer below the P-well layer; and a P-type substrate below the deep N-well layer. The motivation for doing so, as is taught by Kim et al., is reducing defects in the circuit devices (col. 1, paragraph [0002]). Therefore, it would have been

obvious to combine Kim et al. with Karp et al. to obtain the invention of claims 4, 11 and 19.

Allowable Subject Matter

8. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 20-21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a one-time programming memory element comprising a capacitor having an oxide layer capable of passing direct gate tunneling current; a write circuit comprising a first switch connected between a first terminal of said capacitor and a first voltage, and second switch transistor connected between a second terminal of said capacitor opposing said first terminal and a second voltage; and a read switch including plural transistors coupled to said capacitor, wherein the capacitor is one-time programmable as an antifuse.

Response to Arguments

11. Applicant's arguments with respect to claims 1-14, 17-19, and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD

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